

Dr. Sanatan Chattopadhyay

Sanatan Chattopadhyay, MSc, PhD, PGCAP(UK)

Associate Professor

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Educational Qualifications:

PGCAP (2004): University of Newcastle upon Type, UK.

Ph. D. (1999): Major: Microelectronics; Jadavpur University, Calcutta and I.I.T. Kharagpur.
Thesis: *Studies on Optoelectronic Applications of SiGe Alloys*.

M. Sc.: (1994): Electronic Science; University of Calcutta, Calcutta.

B. Sc. (1992): Physics Hons. (with Maths. and Chemistry); University of Calcutta, Calcutta.

Work Experience:

Lecturer (Oct 2003 - Mar 2007): School of Electrical, Electronics and Computer Engineering,
University of Newcastle upon Tyne, United Kingdom.

Research Associate (Feb 2001 – Oct 2003): School of Electrical, Electronics and Computer
Engineering, University of Newcastle upon Tyne, United Kingdom.

Post-Doc Fellow (March 1999 - Feb 2001): Singapore (NUS) - MIT (USA) Alliance (SMA).

Academic Activities:

1. Project Funds Attracted :

- *Design and implementation of digital microfluidic based chips for Bio-medical Applications*, (Phase I: **Rs. 1.0 Crore**; Completed). Funded by: WBDITE. (Co-PI).
- *Design and implementation of digital microfluidic based chips for Bio-medical Applications*, (Phase II: **Rs. 1.46 Crores**, Ongoing) Funded by: WBDITE. (PI).
- Development of **Center of Excellence (COE)** entitled *Systems Biology and Biomedical Engineering* (Phase I: **Rs. 5.0 Crores**, Completed). Funded by: World Bank, TEQIP Phase-II. (CO-PI).
- Development of **Center of Excellence (COE)** entitled *Systems Biology and Biomedical Engineering* (Phase II: **Rs. 4.0 Crores**, Ongoing); Funded by: World Bank, TEQIP Phase - III). (CO-PI).
- *Point-of-care Electronic Diagnosis of Anemic Diseases by Employing Impedimetric Techniques*; (**Rs. 69 Lakhs**, Ongoing); Funded by: DST SERB (CO-PI).
- *Technology-aware modelling and implementation of single, two and multi qubit*

quantum operations for Quantum nanostructures including Quantum Dots (QDs) and Nanowires (NWs); (Rs. 2.0 Crores; Sanctioned). (PI).

- *Growth and characterization of Si/Ge nanowire*; (**Rs. 2.0 Lakhs + 3 years fellowship;** Completed); Funded by: CRNN, C. U. (UGC)
- *Modeling and characterization of process induced strain in nanoscale CMOS*; (**Rs. 2.0 Lakhs + 3 years fellowship;** Completed); Funded by: CRNN, C. U. (UGC).
- *EDA tools for strained Si CMOS cell libraries with variability models*, £160,000.00; Funded by: EPSRC (UK). (PI).
- *Strained Si/SiGe: Materials, Technology and Design*, (£440,000.00; Completed); Founded by: EPSRC (UK). (Co-PI).
- *Strained Si/SiGe VS Heterojunction Bipolar Transistor (HBT)*, (£400,000.00; Completed); Founded by: EPSRC (UK). (Co-PI)
- *SiGe for MOS Technologies 2*; (£400,000.00; Completed); Funded by: EPSRC (UK). (Principal Researcher).

2. Ph.D. and Project Supervision:

- Ph. D. Supervised: Awarded: 13 (3 UK); Continuing: 6.
- M. Phil.: 1 (UK).
- M. Tech. Project: 5.
- M. Sc. Project: 60 (8 UK).
- B. Eng.: 10 (UK).

3. Publication Highlights

3.1 Books:

- C. K. Maiti, S. Chattopadhyay and L K Bera: *Strained-Si Heterostructure Field Effect Devices*; Taylor & Francis, ISBN: ISBN 9780750309936 (2007).
- H. Rahman, S. Chattopadhyay and S. Chattopadhyay: *Progress in VLSI Design and Test (Edited Book), Proceedings of 16th International Symposium on VLSI Design and Test, VDAT 2012*, Springer, ISBN: 9783642314933 3642314937.

3.2 Book Chapters:

1. J. Sultana, S. Paul, A. Karmakar, and S. Chattopadhyay: *Investigating the growth-time dependent comparative performance of vapour-liquid-solid (VLS) grown p-CuO/n-Si thin film hetero-junction solar cells*, *Advances in Optical Science and Engineering* (2017); ISBN: 978-981-10-3907-2; pp. 157-164.
DOI:10.1007/978-981-10-3908-9_18
2. S. Sikdar, B. Nag Chowdhury, and S. Chattopadhyay: *Designing InP-nanowire based vertical metal-oxide-semiconductor capacitors for wavelength selective visible light sensing*, *The Physics of Semiconductor Devices*, ISBN: 978-3-319-97603-7pp. vo. 215, pp 957-962 (2017).
DOI: 10.1007/978-3-319-97604-4_145

3. S. Sikdar, B. Nag Chowdhury, and S. **Chattopadhyay**: *Analytical modeling of vertically oriented standalone Si-Nanowire metal – oxide - semiconductor capacitors for wavelength selective near-infrared sensing applications, Advances in Optical Science and Engineering*, ISBN: 978- 981-10-3907-2; pp. 173-179 (2017).
DOI:10.1007/978-981-10-3908-9_20.
4. R. Saha, A. Das, A. Karmakar, N.R. Saha, ans S. **Chattopadhyay**: *Investigation of oxygen vacancy induced resistive switching memory behavior in low-temperature grown n-ZnO/p-Si heterojunction diode, Computational Science and Engineering, Taylor & Francis Group*, ISBN 978-1-138-02983-5, pp. 225-229 (2017).
5. J. Sultana, S. paul, A. karmakar, and S. **Chattopadhyay**: *Studying the comparative performance of p-CuO/n-Si thin film hetero-junction solar cells grown by Chemical Bath Deposition and Vapor Liquid Solid processes, Computational Science and Engineering, Chapter: Heterojunction devices and circuits; Taylor and Francis, (2016)*; ISBN: 978-1-138-02983-5.
6. J. Sultana, S. Paul, A. Karmakar, and S. **Chattopadhyay**: *Investigating the growth-time dependent comparative performance of Vapor Liquid Solid (VLS) grown p- CuO/n-Si thin film hetero-junction solar cells, Advances in Optical Science and Engineering (2016): Chapter: Green Photonics: Applied Photovoltaics, Application of Solar Energy, Organic Photovoltaics; Springer Singapore., ISBN: 978-981-10-3908-9*.
DOI:10.1007/978-981-10-3908-9.
7. S. Paul, J. Sultana, A. Karmakar, S. **Chattopadhyay**, P. Singha, and A. Banerjee: *Electrical characterization of n-ZnO/p-CuO thin film hetero-junction solar cell grown by chemical bath deposition and vapor liquid solid technique with varying reaction time.* (2016).
DOI:10.1007/978-981-10-3908-9_19.
8. S. **Chattopadhyay**, S. Chakraborty, C. Das, and R. Saha: *Recent progresses on micro- and nano-scale electronic biosensors: A review, Nanospectrum: A Current Scenario (2015): Chapter 5: pp. 19-40; Allied Publishers Pvt. Ltd.*, ISBN: 978-93-85926-06-8.
9. K. Mukherjee, S. Upreti, A. Bag, S. Mallik, M. Palit, and S. **Chattopadhyay**, C. K. Maiti: *Resistive switching in MIM capacitors using porous anodic alumina (2013): Chapter 8: pp. 29-32; Springer International Publishing., ISBN: 9783319030012*.
DOI:10.1007/978-3-319-03002-9_8.
10. S. Upreti, K. Mukherjee, M. Palit, A. Bag, S. Mallik, S. **Chattopadhyay**, and C. K. Maiti: *Porous anodic alumina template formation: deposition technique dependence;* (2013): Chapter 187: pp. 725-728; Springer International Publishing.
ISBN: 9783319030012.

DOI:10.1007/978-3-319-03002-9_187.

3.3 Publications in peer review Journals:

1. B. Chakraborty, R. Saha, **S. Chattopadhyay**, D. De, R. D. Das, M. K. Mukhopadhyay, M. Palit, and C. RoyChaudhuri: *Impact of surface defects in electron beam evaporated ZnO thin films on FET biosensing characteristics towards reliable PSA detection*, **Applied Surface Science 537**, p. 147895 (2021).
DOI: 10.1016/j.apsusc.2020.147895.
2. S. Paul, J. Sultana, N. R. Saha, G. Dalapati, A. Karmakar, and **S. Chattopadhyay**: *Impact of seed layer annealing on the optoelectronic properties of double-step CBD grown n-ZnO nanowires/p-Si heterojunctions*, **Optik 228**, p. 166141 (2020).
DOI: 10.1016/j.ijleo.2020.166141.
3. M. Palit, B. Nag Chowdhury, S. Sikdar, K. Sarkar, P. Banerji, and **S. Chattopadhyay**: *Band splitting induced by momentum-quantization in semiconductor nanostructures: observation of emission lines in Indium Phosphide (InP) nanotubes*, **Physics Letters A 388C**, p. 127056 (2020).
DOI: 10.1016/j.physleta.2020.127056
4. C. Das, B. Nag Chowdhury, S. Chakraborty, S. Sikdar, R. Saha, A. Mukherjee, A. Karmakar, and **S. Chattopadhyay**: *A diagrammatic approach of impedimetric phase angle-modulus sensing for identification and quantification of various polar and non-polar/ionic adulterants in milk*, **LWT- Food Science and Technology 136**, p. 110347 (2020).
DOI: 10.1016/j.lwt.2020.110347.
5. S. Chakraborty, S. Das, C. Das, S. Chandra, K. Das Sharma, A. Karmakar, and **S. Chattopadhyay**: *On-chip estimation of hematocrit level for diagnosing anemic conditions by impedimetric techniques*, **Biomedical Microdevices 22**, p. 38 (2020)
DOI: 10.1007/s10544-020-00493-5.
6. R. Saha, A. Karmakar, and **S. Chattopadhyay**: *Enhanced self-powered ultraviolet photoresponse of ZnO nanowires/p-Si heterojunction by selective in-situ Ga doping*, **Optical Materials**, 105, pp. 109928 (2020).
DOI.org/10.1016/j.optmat.2020.109928.
7. S. Kanungo, B. Majumdar, S. Mukhopadhyay, D. Som, **S. Chattopadhyay**, and H. Rahaman: *Investigation on the Effects of Substrate, Back-Gate Bias and Front-Gate Engineering on the Performance of DMTFET based Biosensors*, **IEEE Sensors Journal 20**, pp. 10405 - 10414 (2020).
DOI: 10.1109/JSEN.2020.2994295

8. R. Bose, R. Saha, **S. Chattopadhyay**, and R. Pal: *Utilization of nanoporous biosilica of diatoms as a potential source material for fabrication of nanoelectronic device and their characterization*, *Journal of Applied Phycology* **32**, pp. 3041–3049 (2020).
DOI:10.1007/s10811-020-02134-z.
9. J. Sultana, S. Paul, R. Saha, S. Sikdar, A. Karmakar, and **S. Chattopadhyay**: *Optical and electronic properties of chemical bath deposited p-CuO and n-ZnO nanowires on silicon substrates: p-CuO/n-ZnO nanowires solar cells with high open-circuit voltage and short-circuit current*, *Thin Solid Films*, **699**, p. 137861 (2020).
DOI: 10.1016/j.tsf.2020.137861
10. A. Bhattacharya, J. Sultana, S. Sikdar, R. Saha, and **S. Chattopadhyay**: *Investigating the impact of thermal annealing on the photovoltaic performance of chemical bath deposited SnO₂/p-Si heterojunction solar cells*, *Microsystem Technologies* **26**, pp. 1351-1358 (2020).
DOI: 10.1007/s00542-019-04667-x.
11. A. Adhikari, S. De, D. Rana, J. Nath, D. Ghosh, K. Dutta, S. Chakraborty, **S. Chattopadhyay**, M. Chakraborty, and D. Chattopadhyay: *Selective sensing of dopamine by sodium cholate tailored polypyrrole-silver nanocomposite*, *Synthetic Metals* **260**, pp. 116296 (2020).
DOI: 10.1016/j.synthmet.2020.116296
12. C. Das, S. Chakraborty, N. K. Bera, D. Chattopadhyay, A. Karmakar, and **S. Chattopadhyay**: *Quantitative estimation of soda ash as an adulterant in aqueous sucrose solution by employing electrical impedance and capacitance spectroscopy*, *Measurement* **148**, pp. 106937 (8 pages), (2019).
DOI: 10.1016/j.measurement.2019.106937
13. R. Saha, S. Sikdar, B. N. Chowdhury, A. Karmakar, and **S. Chattopadhyay**: *Catalyst-modified vapor-liquid-solid (VLS) growth of single crystalline β-Gallium Oxide (Ga₂O₃) thin film on Si-substrate*, *Superlattices and Microstructures*, **136**, p. 106316 (2019).
DOI:10.1016/j.spmi.2019.106316.
14. J. Sultana, A. Bhattacharya, A. Karmakar, G. K. Dalapati, and **S. Chattopadhyay**: *Graphene - nanoparticle incorporated responsivity tuning of p-CuO/n-Si-based heterojunction photodetectors*, *Bulletin of Materials Science* **42**, p. 194 (2019).
DOI:10.1007/s12034-019-1881-6
15. S. Sikdar, B. N. Chowdhury, **S. Chattopadhyay**: *Understanding the electrostatics of top-electrode vertical quantized Si nanowire metal-insulator-semiconductor (MIS) structures for future nanoelectronic applications*, *Journal of Computational Electronics* **18**, pp. 465-472 (2019).

DOI: 10.1007/s10825-019-01321-7

16. S. Chakraborty, C. Das, K. Ghoshal, M. Bhattacharyya, A. Karmakar, and **S. Chattopadhyay**: *Low frequency Impedimetric cell counting: analytical modeling and measurements*, **IRBM 41**, pp. 23-30 (2019).
DOI: 10.1016/j.irbm.2019.07.003
17. S. Roy Barman, S. Chakraborty, A. Mukhopadhyay, and **S. Chattopadhyay**: *Optical analysis authenticated electrical impedance based quantification of aqueous naphthalene*, **Brazilian Journal of Analytical Chemistry 5**, pp. 30-39 (2019).
DOI: 10.30744/brjac.2179-3425.2018.5.20.30-39
18. S. Sadhukhan, T. K. Ghosh, I. Roy, D. Rana, A. Bhattacharyya, R. Saha, **S. Chattopadhyay**, S. Khatua, K. Acharya, and D. Chattopadhyay: *Green synthesis of cadmium oxide decorated reduced graphene oxide nanocomposites and its electrical and antibacterial properties*, **Materials Science and Engineering: C 99**, pp. 696-709 (2019).
DOI:10.1016/j.msec.2019.01.128
19. R. Saha, N. R. Saha, A. Karmakar, G. K. Dalapati, and **S Chattopadhyay**: *Generation of oxygen interstitials with excess in situ Ga doping in chemical bath deposition process for the growth of p-type ZnO nanowires*, **Journal of Materials Science: Materials in Electronics 30**, pp. 8796-8804 (2019).
DOI:10.1007/s10854-019-01204-4.
20. C. Das, S. Chakraborty, N. K. Bera, K. Acharya, D. Chattopadhyay, A. Karmakar, and **S. Chattopadhyay**: *Impedimetric approach for estimating the presence of metanil yellow in turmeric powder from tunable capacitance measurement*, **Food Analytical Methods 12**, pp. 1017-1027 (2019).
DOI:10.1007/s12161-018-01423-1.
21. S. Chatterjee, S. Sikdar, B. Nag Chowdhury, and **S. Chattopadhyay**: *Investigation of the performance of strain-engineered silicon nanowire field effect transistors (ε -Si-NWFET) on IOS substrates*, **Journal of Applied Physics 125**, pp. 082506 (2019).
DOI:10.1063/1.5051310.
22. A. Das, B. Nag Chowdhury, R. Saha, S. Sikdar, J. Sultana, G. K. Dalapati, and **S. Chattopadhyay**: *Formation of high-pressure phase of Titanium Dioxide (TiO_2 -II) thin films by vapor-liquid-solid growth process on GaAs substrate*, **Physica Status Solidi 216**, pp. 1800640 (2018).
DOI:10.1002/pssa.201800640.
23. A. Adhikari, S. De, A. Halder, S. Pattanayak, K. Dutta, D. Mondal, D. Rana, R. Ghosh, N. K. Bera, **S. Chattopadhyay**, M. Chakraborty, D. Ghoshal, and D. Chattopadhyay:

Biosurfactant tailored synthesis of porous polypyrrole nanostructures: A facile approach towards CO₂ adsorption and dopamine sensing, Synthetic Metals **245**, pp. 209-222 (2018).

DOI:10.1016/j.synthmet.2018.09.005.

24. G. K. Dalapati, S. Guhathakurata, A. Das, C. Mahata, S. Chakraborty, S. Bhunia, H. L. Seng, **S. Chattopadhyay**, L. K. Bera, and S. Tripathy: *Suppression of Ge-based defects and auto-doping of p-type epitaxial GaAs by employing Al_{0.3}Ga_{0.7}As bi-layer buffer, Journal of Alloys and Compounds* **765**, pp. 994-1002 (2018).
DOI:10.1016/j.jallcom.2018.06.297
25. A. Mondal, S. Pal, A. Sarkar, T. S. Bhattacharya, A. Das, N. Gogurla, S. K. Ray, P. Kumar, D. Kanjilal, K. D. Devi, A. Singha, **S. Chattopadhyay**, and D. Jana: *Raman spectroscopic analysis on Li, N and (Li,N) implanted ZnO, Materials Science in Semiconductor Processing* **80**, pp. 111-117 (2018).
DOI:10.1016/j.mssp.2018.02.026.
26. J. Sultana, S. Paul, A. Karmakar, G. K. Dalapati, and **S. Chattopadhyay**: *Optimizing the thermal annealing temperature: Technological route for tuning the photo-detecting property of p-CuO thin films grown by chemical bath deposition method, Journal of Materials Science: Materials in Electronics* **29**, pp. 12878–12887 (2018).
DOI:10.1007/s10854-018-9407-3.
27. A. Das, B. Nag Chowdhury, R. Saha, S. Sikdar, S. Bhunia, and **S. Chattopadhyay**: *Ultrathin Vapor–Liquid–Solid grown Titanium Dioxide-II film on bulk GaAs substrates for advanced metal–oxide–semiconductor device applications, IEEE Transactions on Electron Devices*; **65**, pp. 1466-1472 (2018).
DOI:10.1109/TED.2018.2802490.
28. S. Paul, J. Sultana, A. Bhattacharyya, A. Karmakar, and **S. Chattopadhyay**: *Investigation of the comparative photovoltaic performance of n-ZnO nanowire/p-Si and n-ZnO nanowire/p-CuO heterojunctions grown by chemical bath deposition method, Optik - International Journal for Light and Electron Optics*; **164**, pp. 745-752, (2018). DOI:10.1016/j.ijleo.2018.03.076.
29. S. Ray, S. Sen, A. Das, A. Bose, A. Bhattacharyya, A. Das, **S. Chattopadhyay**, S. S. Singha, A. Singha, H. K. Patra, and A. K. Dasgupta: *Bioelectronics at graphene–biofilm interface: Schottky junction formation and capacitive transitions, Medical Devices & Sensors* **1**, pp. e10013 (2018).
DOI: 10.1002/mds3.10013.
30. A. Das, R. Saha, S. Guhathakurata, S. Pal, N. R. Saha, H. S. Dutta, A. Karmakar, and **S. Chattopadhyay**: *Tuning of transport properties of the double-step chemical bath*

- deposition grown zinc oxide (ZnO) nanowires by controlled annealing: An approach to generate p-type ZnO nanowires, Thin Solid Films* **649**, pp. 129-135 (2018). DOI:10.1016/j.tsf.2018.01.036.
31. R. Saha, A. Das, A. Karmakar, and **S. Chattopadhyay**: *Self-rectifying threshold resistive switching based non-volatile memory of CBD/CBD grown vertical n-ZnO nanowire/p-Si heterojunction diodes, Advanced Materials Proceedings* **3**, pp. 298-303 (2018).
32. S. Pal, N Gogurla, A. Das, S. S. Singha, P. Kumar, D. K. Kanjilal, A. Singha, **S. Chattopadhyay**, D. Jana, and A. Sarkar: *Clustered vacancies in ZnO: Chemical aspects and consequences on physical properties, Journal of Physics D Applied Physics* **51**, pp. 105107 (2018). DOI:10.1088/1361-6463/aaa992.
33. S. Chatterjee and **S. Chattopadhyay**: *Fraction of insertion of the channel Fin as performance booster in Strain-Engineered p-FinFET devices with Insulator-on-Silicon substrate, IEEE Transactions on Electron Devices* **99**, pp 1-8 (2017). DOI:10.1109/TED.2017.2781264.
34. J. Sultana, S. Paul, A. Karmakar, and **S. Chattopadhyay**: *Efficiency enhancement of p-CuO/n-Si heterojunction solar cells: impact of annealing on the photovoltaic properties of Vapour-Liquid-Solid (VLS) grown ultra-thin CuO film, Materials today proceedings* **4**, pp. 12694-12697 (2017). DOI:10.1016/j.matpr.2017.10.085.
35. S. Paul, J. Sultana, A. Karmakar and **S. Chattopadhyay**: *Effect of prolonged growth on the chemical bath deposited ZnO nanowires and consequent photovoltaic performance of n-ZnO NWs/p-CuO heterojunction solar cells, Materials today proceedings* **4**, pp. 12496-12499 (2017). DOI:10.1016/j.matpr.2017.10.050.
36. A. Ghosh, J. Sinha, and **S. Chattopadhyay**: *A comparative study on the performance of RESET based electro-thermal process in ring shaped confined Ge₂Sb₂Te₅ and Ge₁Cu₂Te₃ chalcogenide memory structures, Materials Today Communications* **13**, pp. 325-331 (2017). DOI:10.1016/j.mtcomm.2017.10.017.
37. K. Ghoshal, S. Chakraborty, C. Das, **S. Chattopadhyay**, S. Chowdhury, and M. Bhattacharyya: *Dielectric properties of plasma membrane: A signature for dyslipidemia in diabetes mellitus, Archives of Biochemistry and Biophysics* **635**, pp. 27-36 (2017). DOI:10.1016/j.abb.2017.10.002.
38. S. Kanungo, S. A. Mondal, **S. Chattopadhyay**, H. Rahaman: *Design and investigation*

on Bio-Inverter and Bio-Ring-oscillator for dielectrically modulated biosensing applications, IEEE Transactions on Nanotechnology 16, pp. 974-981 (2017).
DOI:10.1109/TNANO.2017.2736161.

39. T. K. Ghosh, S. Sadhukhan, D. Rana, G. Sarkar, C. Das, **S. Chattopadhyay**, D. Chattopadhyay, and M. Chakraborty: *Treatment of recycled cigarette butts (man-made pollutants) to prepare electrically conducting material*, *Journal of Indian Chemical Society* **94**, pp. 863-870 (2017). 94(8):863-870.
40. K. Sarkar, M. Palit, S. Guhathakurata, **S. Chattopadhyay**, and P. Banerji: *Single $In_xGa_{1-x}As$ nanowire/p-Si heterojunction based nano-rectifier diode*, *Nanotechnology* **28**, p. 385202 (2017).
DOI:10.1088/1361-6528/aa7f19.
41. K. Sinha, **S. Chattopadhyay**, P. S. Gupta, H. Rahaman: *A technique to incorporate both tensile and compressive channel stress in Ge FinFET architecture*, *Journal of Computational Electronics* **16**, p p . 620 - 630 (2017).
DOI: 10.1007/s10825-017-1003-x.
42. C. Das, S. Chakraborty, K. Acharya, N. K. Bera, D. Chattopadhyay, A. Karmakar, and **S. Chattopadhyay**: *FT-MIR supported Electrical Impedance Spectroscopy based study of sugar adulterated honeys from different floral origin*, *Talanta* **171**, pp. 327-334 (2017).
DOI:10.1016/j.talanta.2017.05.016.
43. M. Palit, B. Nag Chowdhury, A. Das, S. Das, and **S. Chattopadhyay**: *Selective strain incorporation and retention into Si-substrate through VLS growth of TiO_2 nano-islands*, *Materials Research Express* **4**, p. 025005 (2017).
DOI:10.1088/2053-1591/aa5864.
44. S. Chakraborty, C. Das, N. K. Bera, D. Chattopadhyay, A. Karmakar, and **S. Chattopadhyay**: *Analytical modelling of electrical impedance based adulterant sensor for aqueous sucrose solutions*, *Journal of Electroanalytical Chemistry* **784**, pp. 133-139 (2017).
DOI:10.1016/j.jelechem.2016.11.055.
45. S. Chatterjee and **S. Chattopadhyay**: *Analytical modeling of the lattice and thermo-elastic coefficient mismatch-induced stress into silicon nanowires horizontally embedded on insulator-on-silicon substrates*, *Superlattices and Microstructures* **101**, pp. 384-396 (2017).
DOI:10.1016/j.spmi.2016.12.001.
46. A. Ghosh, A. Mondal, A. Das, **S. Chattopadhyay**, K. K. Chattopadhyay: *Removal of oxygen related defects from chemically synthesized In_2O_3 thin film doped with Er by*

spin-on technique, *Journal of Alloys and Compounds* **695**, pp. 1260-1265 (2016).

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47. J. Sultana, S. Paul, A. Karmakar, R. Yi, G. K. Dalapati, and **S. Chattopadhyay**: *Chemical bath deposited (CBD) CuO thin films on n-silicon substrate for electronic and optical applications: Impact of growth time*, *Applied surface science* **418**, pp. 380-387 (2016).
DOI: 10.1016/j.apsusc.2016.12.139.
48. S. Kanungo, **S. Chattopadhyay**, K. Sinha, P. S. Gupta, and H. Rahaman: *A device simulation-based investigation on dielectrically modulated fringing field-effect transistor for biosensing applications*, *IEEE Sensors Journal* **17**, pp. 1399-1406 (2016). DOI:10.1109/JSEN.2016.2633621.
49. S. Sikdar, B. Nag Chowdhury, A. Ghosh, and **S. Chattopadhyay**: *Analytical modeling to design the vertically aligned Si-nanowire metal-oxide-semiconductor photosensors for direct color sensing with high spectral resolution*, *Physica E Low-dimensional Systems and Nanostructures* **87**, pp. 44-50 (2016).
DOI:10.1016/j.physe.2016.10.039.
50. S. Chatterjee and **S. Chattopadhyay**: *Modeling and estimation of process-induced stress in the nanowire field-effect-transistors (NW-FETs) on Insulator-on-Silicon substrates with high-k gate-dielectrics*, *Superlattices and Microstructures* **98**, pp. 194-202, (2016).
DOI:10.1016/j.spmi.2016.08.022.
51. K. Sarkar, M. Palit, **S. Chattopadhyay**, P. Banerji: *An analysis of the growth of silver catalyzed In_xGa_{1-x}As nanowires on Si (100) by metal organic chemical vapor deposition*, *Journal of Applied Physics* **120**, p. 084309 (2016).
DOI:10.1063/1.4961733.
52. P. S. Gupta, H. Rahaman, K. Sinha, and **S. Chattopadhyay**: *An optoelectronic band-to-band tunnel transistor for near-infrared sensing applications: Device physics, modeling, and simulation*, *Journal of Applied Physics* **120**, p. 084510 (2016).
DOI:10.1063/1.4961426.
53. K. Sinha, P. S. Gupta, **S. Chattopadhyay**, and H. Rahaman: *Investigating the performance of SiGe embedded dual source p-FinFET architecture*, *Superlattices and Microstructures*, **98**, pp. 37-45(2016).
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76. L. S. Driscoll, S. Olsen, **S. Chattopadhyay**, A. G. O'Neill, and K. S. K. Kwa: *Impact of Ge diffusion and wafer cross hatching on strained Si MOSFET electrical parameters*, **in the Proc. of Int'l Conference on Materials Research Symposium (MRS)**, San Francisco, USA, (2004).
77. **S. Chattopadhyay**, A. R. Saha, G. K. Dalapati, S. K. Nandi, and C. K. Maiti: *Electrical properties of NiSi/strained-Si Schottky diodes*, **in the Proc. of Int'l Conf. on Computers and Devices for Communication (CODEC 2004)**, Calcutta, (2004).
78. S. H. Olsen, L. S. Driscoll, K. S. K. Kwa, **S. Chattopadhyay**, A. G. O'Neill: *High performance strained-Si/SiGe N-channel MOSFETs: impact of alloy composition and layer architecture*, **Solid State Devices and Materials (2003)**, SSDM, Japan (2003).

79. K. S. K. Kwa, **S. Chattopadhyay**, S. Olsen, L. Driscoll, and A. G. O'Neill: *Optimization of channel thickness in strained-Si/SiGe MOSFETs, European Solid-State Device Research Conference (ESSDERC 2003)*, Estoril, Portugal, (2003).
80. S. Olsen, L. Driscoll, K. S. K. Kwa, **S. Chattopadhyay**, A. O'Neill, A. Waite, Y. Tang, A. Evans, D. Norris, A. Cullis, D. Paul, and D. Robbins: *High performance strained-Si/SiGe n-MOSFETs using a novel CMOS architecture, Proceedings of 3rd Intl. Conf. on Silicon Epitaxy and Heterostructures (ICSI 3)*, Santa Fe, USA, pp. 132-134, (2003).
81. S. H. Olsen, A. G. O'Neill, D. J. Norris, A. G. Cullis, S. J. Bull, **S. Chattopadhyay**, K. S. K. Kwa, L. S. Driscoll, A. M. Waite, Y. T. Tang, and A. G. R. Evans: *Thermal oxidation of strained Si/SiGe: impact of surface morphology and effect on MOS devices, Euro. Mat. Soc. Spring Meeting (E-MRS 2003)*, Strasbourg, France, (2003).
82. S. H. Olsen, A. G. O'Neill, **S. Chattopadhyay**, K. S. K. Kwa, L. S. Driscoll, S. J. Bull, A. M. Waite, Y. T. Tang, A. G. R. Evans, D. J. Norris, A. G. Cullis, and J. Zhang: *Impact of virtual substrate Ge composition on strained Si MOSFET performance, Electronic Materials Conference*, USA (2003).
83. S. H. Olsen, **S. Chattopadhyay**, K. S. K. Kwa, L. S. Driscoll, A. G. O'Neill: *Impact of material quality on high performance strained Si/SiGe heterostructure MOSFETs, 2003 Silicon Nanoelectronics Workshop*, Kyoto, Japan, pp. 34-35, (2003).
84. L. S. Driscoll, A. G. O'Neill, S. H. Olsen, **S. Chattopadhyay**, K. S. K. Kwa: *Dual quantum well strained silicon/silicon-germanium n-channel heterojunction metal oxide field effect transistors for CMOS logic, PREP Conference, PREP 2003*, Exeter, UK, (2003).
85. K. L. Tong, K. L. Pey, W. K. Choi, **S. Chattopadhyay**, E. A. Fitzgerald, and D. Antoniadis: *Schottky barrier heights of Ti on n-type Si_{0.75}Ge_{0.25}, in the proceeding of International Workshop on Advances in Materials Science and Technology*, IMRE, Singapore (2000).
86. **S. Chattopadhyay**, K. L. Pey, W. K. Choi, D. Z. Chi, D. A. Antoniadis, and E. A. Fitzgerald: *Identification of deep level traps in a compositionally graded n-Si_{0.75}Ge_{0.25} alloy using Ti schottky diode, in the proceeding of International Conference on Communications, Computers & Devices (ICCCD-2000)*, I. I. T. Kharagpur (2000).
87. **S. Chattopadhyay**, L. K. Bera, S. K. Ray, P. K. Bose, and C. K. Maiti: *Schottky barrier height of Pt/p-strained-SiGe diodes, in the Proc. of Int'l Conference on Computers and Devices for Communication (CODEC 1998)*, Calcutta, (1998).
88. **S. Chattopadhyay**, L. K. Bera, S. K. Ray, P. K. Bose, and C. K. Maiti: *Low temperature characteristics of Pt/p-strained-Si schottky diodes, in the Proc. of 9th Int'l Workshop on Physics of Semiconductor Devices (IWPSD-98)*, Delhi (1998).
89. **S. Chattopadhyay**, P. K. Bose, and C. K. Maiti: *Spectral response of relaxed Si_{1-x}Ge_x heteroepitaxial p-i-n photodiodes, in the Proc. of Int'l Conference on Fibre Optics and Photonics (PHOTONICS-98)*, IIT Delhi, (1998).

3.6 Publications in Peer Reviewed National Conferences:

1. K. Sinha, **S. Chattopadhyay**, and H. Rahaman: *Strained Silicon – a gateway to a aster world*, National Conference on Advancement in Frontier Physics: From 20th Century to the Present (2016).
2. H. K. Ramakrishnan, **S. Chattopadhyay**, and A. Yakovlev: *Study of impact of variability in CMOS using Monte Carlo simulation*, PGC 2006, (2006).
3. Y. L. Tsang, **S. Chattopadhyay**, and A. G. O'Neill: *Modelling threshold voltage in strained Si n-MOSFET*, PGC 2006 (2006).
4. J. Varzgar, **S. Chattopadhyay**, and A. G. O'Neill: *Characterisation and analysis of deep submicron strained Si mos devices*, PGC 2006 (2006).
5. S. S. Shedable, **S. Chattopadhyay**, and A. Yakovlev: *Study of variability sources and its impact in ic technology*, PGC 2006 (2006).
6. M. O. Alatise, S. H. Olsen, **S. Chattopadhyay**, and A. G. O'Neill: *Capacitance-voltage simulation and characterisation of strained Si/SiGe MOS devices*, PGC 2006 (2006).
7. K. S. Kwa, **S. Chattopadhyay**, A. G. O'Neill, and S. H. Olsen: *Electrical characterisation of strained Si MOS capacitors*, PGC 2005 (2005), p. 25 (2005).
8. H. K. Ramakrishnan, A. Yakovlev, and **S. Chattopadhyay**: *Analysis and comparison of strained Si CMOS inverters against Si*, PGC 2005, p. 26 (2005).
9. J. Varzger, **S. Chattopadhyay**, A. G. O'Neill, K. S. Kwa, and S. H. Olsen: *Analysis and characterisation of strained Si deep submicron MOS devices*, PGC 2005, p. 54 (2005).
10. Y. L. Tsang, **S. Chattopadhyay**, and A. G. O'Neill: *Next generation high-performance MOSFETs on strained Si/SiGe platform*, PGC 2005, p. 53 (2005).
11. R. S. Dhar, **S. Chattopadhyay**, and A. G. O'Neill: *AC conductance technique to eliminate the effect of self-heating in strained-Si/SiGe MOSFET*, PGC 2005, p. 56 (2005).
12. **S. Chattopadhyay**, K. S. K. Kwa, S. H. Olsen, L. S. Driscoll and A. G. O'Neill: *Strained-Si/SiGe C-V characteristics for heterojunction MOSFET channel design*, PGC 2003, (2003).
13. K. S. K. Kwa, **S. Chattopadhyay**, S. H. Olsen, L. S. Driscoll, and A. G. O'Neill: *Model for reconstruction of the C-V characteristics from measured lossy metal-oxide-semiconductor capacitance-voltage characteristics*, PGC 2003, U.K. (2003).
14. S. H. Olsen, L. S. Driscoll, K. S. K. Kwa, **S. Chattopadhyay**, A. G. O'Neill, A. M. Waite, Y. T. Tang, A. G. R. Evans, D. J. Norris, A. G. Cullis, D. J. Paul, and D. J. Robbins: *High performance strained Si/SiGe nMOSFETs using a novel CMOS architecture*, PGC 2003, U.K., (2003).

15. S. Chattopadhyay and A. G. O'Neill: *Thermal reaction during Ni-silicidation with Si_{0.75}Ge_{0.25} alloy*, PGC (2002).
16. S. Chattopadhyay, K. L. Pey, W. K. Choi, H. Zhao, E. A. Fitzgerald, and D. A. Antoniadis: *Characterization of the rapid thermal annealed Ni-silicided films on UHVCVD grown relaxed n-Si_{0.75}Ge_{0.25} epitaxial layer*, 1st Annual Symposium of Singapore-MIT Alliance (SMA Symposium) (2001).
17. H. Zhao, K. L. Pey, S. Chattopadhyay, W. K. Choi, P. S. Lee, E. A. Fitzgerald, and D. A. Antoniadis, J. A. van Kan, T. Ospowitcz, and Z. X. Shen: *Interfacial reaction of Ni on Si_{0.7}Ge_{0.3} at low temperature by rapid thermal annealing*, 1st Annual Symposium of Singapore-MIT Alliance (SMA Symposium) (2001).
18. E. A. Fitzgerald, M. T. Currie, C. W. Leitz, M. Armstrong, G. Taraschi, Z. Y. Cheng, D. A. Antoniadis, C. S. Tan, S. Chattopadhyay, H. Zhao, P. S. Lee, L. Miao, S. J. Chua, K. L. Pey, and W. K. Choi: *The relaxed SiGe materials platform: strained Si MOS*, 1st Annual Symposium of Singapore-MIT Alliance.

4. Some Relevant Information Related to Research:

- News item:
<https://www.innovations-report.com/html/reports/information-technology/report-15857.html>.
- News item:
<https://www.sciencedaily.com/releases/2003/01/030120100124.htm>
- News item:
(CURRENT SCIENCE Vol. 113, No. 4, p. 540-541, 25th August, 2017).

5. Invited Lectures /Session Chairs /Resource Persons:

1. Resource Person: *Science, Technology and Innovation: with an emphasis on its gradual evolution*, 1st Faculty Induction Programme (FIP-01) (Webinar), North Bengal University (2020).
2. *Semiconductor devices: the past, present and future*, International Webinar on Electronic Devices: Past, Present and future, organized by APC College (2020).
3. *MOSFET: the key of modern technology*, Webinar on Applications of Electronics, organized by Vivekananda College, Kolkata (2020).
4. *Utilization of process induced strain for developing high pressure TiO₂-II phase*, International Symposium on Devices, Circuits and Systems (ISDCS) (2020).
5. *Strain engineering for mobility enhanced Metal-Oxide-Semiconductor Field Effect Transistors (ϵ -Si MOSFETs)*, One Day Seminar, Batanagar College (2019).
6. *Channel strain engineering: an effective route for sustaining MOSFET performance*, International Conference, UEM (2019).

7. *High dielectric constant materials (high-k dielectrics) for electronic applications*, International Conference on Innovation in Material Science & Technology (IMST 2018), Organized by Indian Rubber Industry, Kolkata Branch and Amity University.
8. *Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) with Quantum-Scale channel lengths*, IEEE Student Branch, Organized by APC College (2018).
9. *Stress incorporation in nano-scale metal-oxide-semiconductor field effect transistor channels for controlled performance enhancement*, International Symposium on Devices, Circuits and Systems (ISDCS) (2018).
10. *High dielectric constant materials (high-k dielectrics) for electronic applications*, One Day Symposium, UEM (2018).
11. *The challenges and advances of metal-oxide-semiconductor field effect transistors (MOSFETs): a journey of 60 years*, IEEE EDS Society; Organized by Heritage Institute (2017).
12. *Inclusive progress requires holistic approach for the practice of science and technology*, One day Seminar, Mallabhum Institute of Technology (2017).
13. *Nano-dimensions: an additional parameter for designing electronic systems*, Amity University, Kolkata (2017).
14. *Semiconductor devices: the wonder element to direct the path of civilization and social life*, IEEE EDS Society Organized by Heritage Institute (2017).
15. *Challenges in Metal-Oxide-Semiconductor Field Effect Transistors for Developing Low Power Circuits*, Faculty Development Program, JIS College (2017).
16. *Induced elastic stress/strain: the tunable material parameter for performance enhancement in nano-scale electronic devices*, International Conference, NIT Durgapur (2017).
17. *Evolution of CMOS device and technology for low power applications*, International Conference on Microelectronics, Computing and Communication (MicroCom 2016).
18. (Session Chair) *Electrical and Electronic Devices*, IEEE International Conference on Computational Intelligence and Communication Networks (ICCICN 2014).
19. (Session Chair): *Nanomaterials and Devices*, International Conference on Computers and Devices for Communication (CODEC-15).
20. Session Chair: *Demystifying Time Varying Circuits & Systems*, 29th International Conference on VLSI Design, (2012).
21. (Session Chair) *Let There Be Light: A Challenge For Control Engineers (Key note)*, IEEE First International Conference on Control, Measurement and Instrumentation (CMI) (2016).
22. *Some selective applications of engineered beam on electronic material and devices*, National Workshop on the Application of Radiation in Physical, Chemical and Life

Sciences (2013); UGC-DAE Consortium for Scientific Research Kolkata Centre & CRNN, CU.

23. *Nano-electronic devices: useful for developing bio-chips?* Workshop on Nanotechnology and Biochip (2014).
24. *Emerging materials and devices for electronic applications, Emerging Materials & Devices* (EMD- 2014).
25. *Advances in nanotechnology*, National Conference on Recent Development in Electrical, Electronics and Engineering Physics (RDE3P-2013).
26. *Advances in nano-scale technology*, One day Seminar on "Recent trends in Frontier of Physics" (2013).
27. *Low power high speed CMOS devices for VLSI technology*, Seminar on Emerging Technologies in the Field of Electrical, Electronics and Instrumentation Engineering. (2014).
28. (Session Chair): Session: *Device Electronics Track-I*, AICTE sponsored National Conference on control, Communication and Device Electronics N3CD-2013.
29. *Materials for advanced CMOS technology: Evolution and Advances*, Seminar on "Recent Trends in Material Research" (2015).
30. *An Introduction to Nano-electronics and its Applications*, Seminar on Glimses of Advance Physics-2; (2014).
31. Resource Person (Refresher Course): *Nano-scale metal-oxide-semiconductor field-effect-transistors (MOSFETs): Evolution and Advances*, JU (2013).
32. Resource Person (Refresher Course): *Nano-electronics for developing Biochip*, Jadavpur University (2015).
33. Resource Person (Faculty Development Program): *Advances in Microelectronics, VLSI Design and Optoelectronics Devices with Mixed Signal Analysis*, Narula Institute of Technology.
34. Resource person: *VLSI Devices and Circuits*, Instruction Enhancement Programme (IEP) under SMDP-C2SD Mission.
35. *Advancement in Solid State Device Resource Person*, Faculty Development Program, RCC Institute of Information Technology (2014).
36. *Challenges of Moore's law and emergence of Nanowire field effect transistors*, 3 Days' workshop on Emerging and Post-CMOS Technologies, Indian Institute Engineering Science Technology (2014).
37. *Complementary-metal-oxide-semiconductor (CMOS): A 50-year journey of electronics from micro- to nano-scale*, One Day Seminar, Tamluk College (2012).
38. *CMOS: Device physics, Technology, Scaling and Associated Challenges*, Summer School (FabTech.) (2011), IRPE CU.

39. *Potential of strained-Si CMOS for low-power high speed circuit applications*, International Conference ICCCD 2010, IIT Kharagpur (2010).
40. *Modifications of CMOS in nano-dimension*, HMRD Summer School, IIT Kharagpur (2010).
41. *Strained-Si/SiGe systems for low power high speed CMOS applications*, One day Seminar One day Seminar on Semiconductor Devices (2010).
42. *Possibility of optoelectronic integrated circuit (OEIC) for CMOS nanoelectronics*, SPIE Student branch, JIS College Chapter (2010).
43. *SiGe for photonics and optoelectronic integrated circuit (OEIC)*, SPIE Kolkata (2010).
44. Resource person: *Metal-oxide-semiconductor field-effect-transistors (MOSFETs) in nano-scale: evolution, science and technology*, Short-term course, IIT Kharagpur (2012).
45. Resource person: *Towards nanoelectronics: MOSFET scaling and Short Channel Effects (SCE)*, Refreshers course, Department of Physics, CU (2009).
46. *Very Large Scale Integration: Device, Technology and Design challenges*, Computer Society of India (2009).
47. *CMOS VLSI: device, technology and design issues*, Computer Society of India (2009).
48. *Strained-Si CMOS: Advances and Challenges*, MHRD and AICTE Continuing Education Program (CEP), IIT, Kharagpur (2008).
49. *Nano-scale CMOS: Device, Technology and challenges*, UGC Networking Program, (NanoDev) IRPE, CU (2009).
50. *Evolution of Si CMOS: A journey from micro- to nano-dimension with associated challenges*, Faculty Development Program, Techno India College (2009).
51. *CMOS devices: Operation, Applications and Modifications in nano-era*, SemiNano, Summer school, Department of Radio Physics and Electronics, under the UGC Centre for Excellence program (2008).
52. *Challenges of Si CMOS in Nano-dimension*, Short term course, MHRD and AICTE Continuing Education Program (CEP), IIT, Kharagpur.
53. *CMOS in Nano-era: its design challenges*, workshop on the faculty training program undertaken by AICTE (2008).
54. *Very large scale integration (VLSI)*, workshop on the faculty training program, Techno India Group (2008).
55. *CMOS in nano-era: alternatives and challenges*, One Day International Symposia, Saha Institute of Nuclear Physics (2008).
56. *Very Large Scale Integration (VLSI): an overview*, workshop on the faculty training program Techno India College (2008).
57. *Si-based optoelectronic integrated circuit (OEIC)*, MHRD Summer School, IIT Kharagpur.

6. Other Involvements:

- Convener of the ‘Clean Room’: Center for Research in Nanoscience and Nanotechnology (CRNN), CU.
- Member of PG BOS, ECE, Moulana Abul Kalam Azad University of Technology.
- Member of PG BOS, ECE, National Institute of Technology, Mizoram.
- Member of PG Board, Electronic Science, APC College, Barasat State University.
- Member of the UG Board, CU, Department of Electronic Science.
- Member of the IEEE Electron Devices Society (EDS).
- Member of BOS, Belur Vidya Mandir, Computer Science.
- Coordinator of Orientation Program, CU (OP-99).
- Advisory Committee member: Several International & National Conferences.
- Organizing Committee member: Several International & National Conferences.
- Ex-Head of the Department, Department of Electronic Science, CU.
- Ex-UG BOS member, Electronic Science, Narendrapur Ramkrishna Mission.
- Ex-coordinator: Foundation year course, School of Electrical, Electronics and Computer Engineering, University of Newcastle Upon Tyne.